Low temperature zero-level packaging of MEMS

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Abstract

Zero-level packaging technology ensures dicing and handling compatibility of the MEMS device along with low cost by encapsulating the MEMS components using wafer level processing. It is also essential for providing the MEMS with a controlled ambient in a cost-effective way. In order to be compatible with a broad range of MEMS processes, IMEC developed sealing methods with a low temperature budget. Zero-level packaging consists of die-to-wafer or wafer-to-wafer capping using a solder or polymer sealing. The first method is based on the soldering of e.g. SnPb. The second method uses photosensitive BenzoCycloButene as a sealing material. In order to reduce the total thickness of the package, the capping wafer can be thinned. In the “thin film capping” technology, a cap is realized using the deposition of poly-SiGe on top of a sacrificial layer. After etching of access holes, the sacrificial layer is etched. Finally the access holes are closed using an appropriate thin film sealing process. Infrared microbolometers, RF-MEMS switches and other MEMS devices have been capped. The quality of the resulting MEMS zero-level packages is evaluated using shear testing, different leak test methods, outgassing analysis as well as measuring the MEMS device characteristics.

Introduction

Packaging of MEMS is much more demanding than traditional IC packaging. MEMS are in general vulnerable to the handling and contamination that are present during standard dicing and packaging. Hence the protection of the fragile microsystems at an early stage is essential. Moreover, dicing of released devices is not possible as many MEMS devices are sensitive to stiction. After capping of the MEMS featuring gross leak tightness, dicing and further handling can be performed without compromising the yield. In order to function reliable over a long lifetime MEMS often require a controlled ambient, e.g. a specific gas at a given pressure (including vacuum). In this case, a fully hermetic package is required.

Traditional packages that meet these stringent requirements come with high cost. Zero-level packaging meets the above requirements at low cost by encapsulating the MEMS components using wafer level processing. Low-cost zero-level packaging techniques offering hermeticity exist (e.g. anodic bonding), but require high temperature processing and an extremely flat bonding surface. Both requirements are often incompatible with the MEMS temperature budget, e.g. if the latter is post-processed on CMOS.

In order to be compatible with a broad range of MEMS processes, IMEC developed sealing methods with a low temperature budget, which at the same time can handle some topography. A first method uses die-to-wafer (D2W) or wafer-to-wafer (W2W) capping using a solder or polymer sealing. In the second method: “thin film capping”, a cap is realized as a part of the processing of the MEMS device itself.

Fig. 1: Schematic layout of a zero-level package for a MEMS device.
Zero-level capping

As shown in fig. 1, for zero-level capping a two substrate approach is used: a wafer with the MEMS devices processed (bottom wafer), and a capping wafer or die, in which a cavity can be etched using e.g. KOH etching. On one (or both) of the top and bottom wafers a sealing ring is deposited (and patterned). The package is then assembled using a flip-chip bonder or a wafer-to-wafer bonder. During the assembly process a controlled temperature is maintained and a force applied. The flip-chip technique provides a die to wafer method, while using the wafer-to-wafer bonder several packages are assembled in one process step. Optionally, a reflow of the seal can be done in a separate oven. This procedure enables the evacuation of the zero-level package through an indent in the sealing ring before the final reflow. This patented “Indent Reflow Sealing” method allows to package MEMS devices in a well-defined atmosphere at a given pressure [1].

Depending on the need, the capping wafer is thinned to about 100 micron in order to reduce the total thickness of the zero-level package. This can be done on wafer scale using wafer to wafer bonding followed by back grinding of the cap wafer [2]. In another approach a thin wafer is temporally bonded to a carrier wafer, and subsequently diced. After flip-chip on the MEMS wafer, the carrier dies are mechanically removed [3].

Examples of MEMS packaging using zero-level technology are shown in Fig. 2. Infrared microbolometers [4], RF-MEMS switches [5] as well as other MEMS devices have been successfully capped.

Solder & polymer sealing

Two different sealing methods are used: one based on low temperature solder, and the other on polymer bonding. The first method is based on the eutectic soldering of SnPb and Ni/Au (Fig. 3) [6]. The layers are deposited using electroplating at both the top (typically SnPb) and bottom wafer (Ni/Au). Other (lead-free) solder seal materials such as In/Au and Sn/Au are being investigated.

The second method uses BenzoCycloButene (BCB) as a sealing material [2,3,7]. BCB is an insulator, thus no extra insulating layer on top of the electrical feedthroughs is needed. Using photosensitive BCB, one of the two wafers can be patterned easily.

Both sealing methods require a maximum temperature budget (240°C) during the flip-chip and eventual reflow. Using this type of sealing is important in terms of the limited temperature budget some MEMS devices feature. Moreover, as opposed to wafer bonding techniques, both the solder and the BCB material can reflow over a limited topography on the MEMS wafer (e.g. electrical feedthroughs) during the reflow process.
Thin film capping

The thin film encapsulation method developed in IMEC is using Plasma Enhanced Chemical Vapour Deposition (PECVD) of poly-SiGe on top of a sacrificial layer. The use of PECVD (instead of LPCVD) results in a reasonable growth rate of 100-200 nm/min even at a low process temperature (520°C). Using this technique cap layers up to 10 micron are grown. After etching of access holes, the sacrificial layer is etched. Finally the access holes are closed using an appropriate thin film sealing process [8]. Caps have been successfully fabricated, encapsulating surface micromachined structures [9]. The advantage of this technique is the use of a wafer scale batch process. Combined with the small area consumed by the package, a low cost solution for zero-level packaging is obtained.
Mechanical & hermeticity testing

The mechanical quality of zero-level packages is tested using shear tests. Both for BCB and solder sealing rings high shear strengths (in the order of 10 MPa) have been obtained. For a typical package of a few square millimeter with a sealing ring width of 300 micron, this corresponds to a force of several kilogram needed to shear the cap off. Hermeticity of packages is tested according to the military standard MIL-STD-883D. It consists of a combination of gross leak and fine leak tests. However, we found out that the combination of a negative gross and fine leak test is no guarantee for full hermeticity [6]. Therefore, new methods are used to test the hermeticity of the sealing. The first test is using a through wafer hole in the MEMS or cap wafer (Fig. 5). When attached to a pumping line using a standard O-ring, the package can be connected to a He leak detector. Using this equipment one is able to detect leak rates down to a few times $10^{-8}$ mbar-l/s up to $10^{-1}$ mbar-l/s [2].

The ultimate test is of course an in-situ pressure measurement using a MEMS device. Surface micromachined infrared microbolometers establish a nice pressure dependence of their thermal conductivity. This feature is used to monitor the pressure inside a zero-level package as a function of time and external pressure [7].

Outgassing of the substrates and sealing materials might influence the MEMS component characteristics. Therefore the outgassing of different materials is being investigated using a Quadrupole Mass Spectrometer.

![Fig. 5: Picture (left) and scheme (right) of the through-hole hermeticity test method.](image)

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