A Circuit Design for Remote Structural Health Monitoring

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ABSTRACT

Intelligent piezoelectric materials are helpful for monitoring the structural health. The principle of the piezoelectric impedance-based structural health monitoring (SHM) technique is to measure the electrical impedance of a piezoelectric patch attached to a structure in a certain frequency range. Electrical impedance variations indicate physical changes in the structure indirectly due to coupling between the electrical and mechanical impedances. This paper presents a circuit design which includes an impedance-based SHM circuits with wireless communication interface. The objective of this research is to develop a new hardware implementation which can be integrated using Very Large Scale Integration (VLSI) techniques for further reduction on the device dimension and power dissipation. It is hoped that both piezoelectric patch and instrumentation device can be attached to a structure with telecommunication capability. The structural integrity can be monitored and the measurement can be acquired and processed at a remote terminal in a real-time manner.

1. INTRODUCTION

Systems and structures which are able to monitor their own structural integrity in operations are becoming an active research field. In traditional methods, both Non-Destructive Evaluation (NDE) and Non-Destructive Testing (NDT) techniques using ultrasonic wave and X-radiography were developed [1–2]. But some researchers paid more attention to damping mechanism in composite materials [3], because natural frequencies, curvature mode shapes, and strain energy mode shapes were proved available to identify damages in a structure. In addition, modal damping deviation based damage detection technique was developed. Other research groups used Lamb-wave to locate structural defects and obtain information about damage type, direction, and severity etc. Meanwhile, Sundaresan et al. argued the use of Scanning Laser Doppler Vibrometer (SLDV) and piezoelectric materials in distributed sensing in 2001 [3]. A review of vibration-based structural health monitoring with special emphasis on composite materials were presented by Montalvao et al. in 2006 [4]. Although vibration-based structural health monitoring is effective in damage detection, the direct access, bulky instrumentation equipment and significant maintenance cost make the on-field monitoring in a structure unfeasible.

Thus, an application of impedance measurements in structural health monitoring was proposed in 1994 [5–7]. In the beginning, the expensive impedance analyzer was used to verify the electromechanical coupling in composite specimen [8]. Then, a more concise resistor capacitor (RC) bridge circuit was built and tested using a high speed Data Acquisition (NI-DAQ) board and LabVIEW software from National Instruments [9]. Then, an operational amplifier based device was developed to record the electrical impedance of piezoelectric patch with Fast Fourier Transform (FFT) algorithm [10]. In 2003, Park et al. presented an overview of piezoelectric impedance-based health monitoring techniques [11–12]. Considering the piezoelectric impedance-based SHM sensors developed to be embedded in remote locations, accessibility is even impossible. Therefore, a reliable communication network between piezoelectric impedance-based sensors and a remote terminal is essential for remote structural health monitoring.

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This paper introduces a new circuit implementation for electrical impedance monitoring on a piezoelectric patch. Considering the sensitivity of specific frequency range in piezoelectric impedance measurements, frequency sweep ranging from 53 kHz to 164 kHz is generated. In addition, 902 MHz to 928 MHz radio frequency (RF) transmitter and receiver modules from LINX Technologies® are employed to construct the serial digital communication with parity check technique.

2. THEORY

2.1 BRIDGE CIRCUIT

The theory behind the circuit design uses a simple Wheatstone bridge circuit. The Wheatstone bridge circuit is used either for measuring or monitoring variations in electrical impedance. A Wheatstone bridge circuit is a symmetric configuration of four elements with known and unknown impedances as shown in Fig. 1.

Elements Z1, Z2, Z3 or Z4, can be any combination of resistors, inductors and capacitors. The bridge circuit is driven by an alternating current (AC) voltage source. If and only if there is no voltage difference between point A and B, the bridge circuit is defined to be balanced. The voltages at points A and B can be evaluated as

\[ V_A = V_{AM} \cos(\omega t + \phi_A) \]  
\[ V_B = V_{BM} \cos(\omega t + \phi_B) \]

, where \( V_{AM} \) and \( V_{BM} \) are the amplitude of voltages at point A and B, respectively. In addition, \( \omega \), \( \phi_A \) and \( \phi_B \) are frequency and phase of AC voltage source, respectively. Let \( V_A = V_B \), it requires \( V_{AM} = V_{BM} \) and \( \phi_A = \phi_B \). Thus get

\[ I_A Z_3 = I_B Z_4 \]  
\[ I_A (Z_1 + Z_3) = I_B (Z_2 + Z_4) \]

Divide the equation (3) by equation (4) on both sides, which can be reduced to

\[ \frac{Z_1}{Z_3} = \frac{Z_2}{Z_4} \]

If \( Z_4 \) is the only unknown impedance, it can be evaluated by

\[ Z_4 = \frac{Z_2 Z_3}{Z_1} \]

Thus, the electrical impedance of piezoelectric patch on a structure can be monitored by another three elements in the Wheatstone bridge circuit under the balanced condition.
2.2 COMMUNICATION CIRCUIT

The architecture of a generic radio frequency (RF) communication system includes data source, encoding, transmission, reception, decoding, and interpretation, which are shown in Fig. 2.

![Fig. 2. Block diagram of generic RF communication system](image)

In the specific application of structural health monitoring, the data source is a 16-bit parallel digital data generated from the piezoelectric impedance-based SHM circuit. The 16-bit data is configured as an 8-bit word for frequency measurements followed by an 8-bit word for relative impedance measurements. Since, the data source is generally raw and unprotected, encoding the data provides a data package that can ensure data integrity between the transmitter and the receiver in noisy environment. Therefore, the digital data is encoded with a 4-bit start-bit and a 4-bit end-bit with parity check for both frequency and impedance information. Parity check is a simple error detecting code, which is accomplished by evaluating the number of bit ones in a given set of bits. There are two types of parity check including even parity check and odd parity check. In the implemented communication system, odd parity check is used.

3. METHOD

The system architecture of piezoelectric impedance-based remote SHM circuits is shown in Fig. 3. Once the parallel data containing impedance and frequency information is available in SHM circuit, it will be changed to serial data through an interface circuit and fed into a transmitter for communication. At the same times, the data received from the receiver will be processed by an embedded microcontroller unit in Field Programmable Gate Array (FPGA). In the end, the microcontroller will send the decoded data to a terminal through a standard RS232 serial port for additional graphic interpretation. The microcontroller also has the capability to select different RF channels for distributed sensing locations in a single structure.

![Fig. 3. System architecture of piezoelectric impedance-based remote SHM circuit](image)
3.1 PIEZOELECTRIC IMPEDANCE-BASED SHM CIRCUIT

The front-end impedance-based SHM circuit contains a clock generator, a bridge circuit, two peak detectors, a differential amplifier, a window comparator, and a corresponding control circuit. The simplified circuit block diagram is shown in Fig. 4.

![Fig.4. Simplified block diagram of the piezoelectric impedance-based SHM circuit [13]](image)

The clock generator generates a square wave with frequency range from 53 kHz to 164 kHz. The square wave is used as the voltage source of the bridge circuit. Two peak detectors are connected at the points A and B of the bridge circuit to detect the voltage amplitudes. A differential amplifier is used to compare these two amplitudes. A window comparator identifies whether the bridge circuit is balanced or not. The window comparator generates a digital signal '0' for the unbalance and '1' for the balance. If the bridge circuit is unbalanced, the resistance of the digital resistor will continue increasing and clock frequency will be maintained. Once the bridge is balanced, the control circuit will hold and record the value of digital resistor as well as the measurement frequency of clock generator. After all the values are recorded, the control circuit will generate an impulse to reset the digital resistor and increase the frequency of the clock generator to repeat the measurement cycle.

3.2 TRANSMITTER AND RECEIVER CIRCUITS

Data transmission and reception are implemented using high-performance RF transceiver and receiver modules from LINX Technologies®. The uni-directional HP-3 RF transmitter and receiver modules offer complete compatibility and numerous enhancements for cost-effective, high-performance wireless transfer of analog and digital information in the popular 902 MHz to 928 MHz RF band. Besides eight parallel selectable channels, 100 additional serial selectable channels at fixed frequency bands between 902.62 MHz to 927.62 MHz improve the flexibility of remote terminal to choose messages transmitted from different sensing locations [14].

In the transmitter model, a 12 MHz voltage controlled oscillator serves as a precision frequency reference and carrier. Modulating signal is low pass filtered at front-end to limit the bandwidth and directly modulate the carrier. The modulated 12 MHz signal and frequency reference is applied into the Phase Lock Loop (PLL) with which 902 MHz to 928 MHz voltage controlled oscillator (VCO) form a stable frequency synthesizer at the desired radio frequency. The output signal from the PLL is power amplified to increase the transmission power. Finally, the modulated signal is coupled to 50\(\Omega\) antenna load through Band Pass Filter (BPF). The block diagram of transmitter is shown in Fig. 5.

![Fig.5. Block diagram of HP-3 transmitter [15]](image)
To ensure reliable communication between transmitter and receiver, both transmitter and receiver employ Frequency Shift Key (FSK) modulation which has higher performance than On/OFF Key (OOK) modulation in low Signal-to-Noise Ratio (SNR) environment. Thus, approximately 1000ft reliable data transmission maximum 56Kbps data rate can be obtained which are sufficient for piezoelectric impedance-based structural health monitoring circuit.

In the double conversion receiver module, the single-end radio frequency (RF) port is matched to 50Ω antenna. RF signal from the antenna is filtered by a surface acoustic wave (SAW) filter to attenuate unwanted adjacent RF bands. SAW filter has better performance than other passive or active band pass filter in RF applications. Then, the signal is amplified by a low-noise linear amplifier to increase the receiver sensitivity. Then the signal is mixed with a local oscillator whose frequency is operating at 34.7 MHz below radio frequency to produce the intermediate frequency (IF). The second conversion is achieved by an IF strip which mixes the 34.7 MHz IF with a 24MHz precision crystal oscillator. In the part of demodulation, quadrature demodulator is used to recover the base-band signal from the carrier. The block diagram of receiver is shown in Fig. 6.

In order to select different SHM sensing locations on a single structure, channel serial selection is implemented using communication between a microcontroller embedded in FPGA and the microcontroller embedded in the receiver module. Data is sent synchronously with the Most Significant Bit (MSB) first. The data package consists of a start period, eight data bits, and a stop period. Data is sent through the data line synchronized with the clock line. At first, both the clock and data lines are high. Once the data line goes low, the loading period begins. The loading period is about 25us at least. Then, the clock line goes low and timing begins. For each rising edge of clock line, the setting time and holding time of data line are at least 8 us. After the last bit, both data and clock lines must be tied to high for at least 5 us to latch the serial channel selection data. The total minimum timing required for channel serial selection is 157 us and the detailed timing diagram is shown in Fig. 7.
3.3 EMBEDDED MICROCONTROLLER IN FPGA

Serial received data from receiver is changed back into parallel data by shift-register synchronized with 1 kHz clock, which was divided from a 50 MHz crystal oscillator. Once 8-bit data was shifted into the register, the interrupt scheme in the processor will read in the 8-bit data from the shift register. The processor will be interrupted three times to store the data in the temporary registers of processor successively. Meanwhile, the processor will analyze the received data to detect the location of start-bit and double check the parity bits in the end-bit to make sure the received data is valid instead of corrupted. Once the parity check does not match, the received byte is considered to be errant and discarded. Then processor is waiting for next available data from shift register. The data structure analyzed by the embedded processor in FPGA is shown in Fig. 8.

For data interpretation and post-processing, valid data is displayed on the LCD and transmitted to Hyper-Terminal using Universal Asynchronous Receiver and Transmitter (UART) with 16×8 byte first-input-first-output (FIFO) buffer. All data processing system is synthesized in the Spartan-3E FPGA from Xilinx®, whose architecture is shown in Fig. 9.
4. EXPERIMENT

Considering the different electrical conductivity, an aluminum plate and a wood plate are chose. The purpose of using these materials is to prove the flexibility of implemented system in monitoring structural health of both conductors and insulators.

4.1 EXPERIMENTAL SETUP

The impedance-based structural health monitoring (SHM) circuit is connected with transceiver through interface circuit. Buffers are used in the interface circuit because current sinking capability of shift register overwhelms the current sourcing capability of counters in impedance-based SHM circuits. In addition, buffers can eliminate the interference between digital circuits in the monitoring circuit and analog circuits in the transmitter. 1 kHz clock was generated from a standard 555 timer for the shift register in interface circuits. The load signal impulse for the shift register was generated through standard logic gates. The receiver in the remote location was connected with a terminal through the FPGA.

4.2 EXPERIMENTAL RESULTS

(1) ALUMINUM PLATE

As shown in Fig. 10, a piezoelectric patch is attached to an aluminum plate at one end. The impedance of the undamaged plate is first measured from the receiver. Then, a damaged plate with one 3-mm diameter hole drilled beside the piezoelectric patch was measured from the receiver. The relative impedances of both undamaged and damaged aluminum plates are compared in Fig. 11 with successive measurement frequencies from 53 kHz to 164 kHz.

![Fig. 10 Aluminum plate and piezoelectric patch](image)

![Fig. 11 Comparison of the impedance-frequency curves of the undamaged and damaged aluminum plates by remote SHM circuits](image)

The impedance measured from the output of the receiver is a relative value in hexadecimal format. In order to prove the significant effect of damage on the impedance of aluminum plate, the standard deviation is plotted in the X-Y plane. According to the plot of standard deviation, the magnitudes of impedance are changed significantly at the measurement frequency of 128.3 kHz.
Similarly, a piezoelectric patch is attached to a wood plate as shown in Fig. 12. The impedances of the undamaged and damaged plate with the same dimension as the aluminum one are measured from the receiver. Their relative impedances are compared in Fig. 13. As we can see, the effect of the same damage on the wood plate is not significant as the counterpart on the aluminum plate, but the curve shapes are still drifted at the frequency of 127.9 kHz.

The experimental results prove that the designed impedance-based remote structural health monitoring system works well in monitoring the electrical impedance variations of small structure. On the other side of coin, the specific structural analysis on the damage metrics is beyond the research scope of this paper [17]. Meanwhile, we are doing the integration of the presented circuits and expecting it can be combined with a piezoelectric patch as a SHM sensor node. The convenience of wireless communication improves the monitoring range of structural health and makes the applications of wireless sensor network in structural health monitoring possible.

5. CONCLUSION

Reliable digital communication is constructed between transmitter and receiver modules using parity check and FSK modulation/demodulation techniques. With communication capabilities between piezoelectric impedance based SHM circuit and remote terminal, the accessing range of structural health monitoring is expanded. Although parity check is the easiest error detection code, it is not robust enough for strong interference. Most importantly, significant system power consumption is a bottleneck for limit battery power supply. Thus, piezoelectric vibration based energy harvesting is a possible solution for powering remote structural health monitoring circuit.
6. REFERENCES